Switching Current Ripple Calculation For The Passive Filter Design Of The Grid Connected Inverter

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***Abstract*- For the grid interconnection of distributed power generation sources through the inverters, problem of injected harmonics is an important issue. A common approach for the suppression of such harmonics is to use L-filter as an interface between the grid and inverter. Correct information of maximum switching current ripple is an important parameter for the design of the inductor. This paper discusses a precise approach for the calculation of such a parameter. Calculation is carried out for both, single phase grid connected inverter with PWM switching technique and three phase grid connected inverter with SVM switching technique. Variation of the maximum switching current ripples during different switching periods over the fundamental period of the grid voltage is presented. Peak of these variations give overall maximum switching current ripple. This approach assures the switching current ripples within the considered design value and accurate design of the inductance filter.**

Keywords- Switching current ripple, grid connected inverter, space vector modulation, filter design.

1. INTRODUCTION

Active converters, at the point of common coupling to the grid, are used to improve the power quality of drives and loads. The conventional way to interface these active converters to the grid is through a first order low-pass filter known as L-filter. The equivalent line impedance can be considered as large enough for the harmonics whereas it should ideally be zero for the fundamental frequency component. But these kinds of filters are inefficient, bulky and cannot meet the harmonic requirements for the interconnection of loads to the grid [1-3]. There are multiple constraints to design higher order LCL-filters used in grid connected inverter applications. Basically the filter are used to reduce the high-order harmonics at grid side, but by choosing a wrong filter with a poor design a lower attenuation or even an increase of the distortion compared to the expected standard can happen. In fact filter resonance or saturation of the inductors can happen due to the current harmonics generated by the converter [4-8]. Hence, design of the filter should be correctly done considering many constraints, such as attenuation of switching harmonic, current ripple through inductors, resonance phenomenon, reactive power of the filter capacitors and total impedance of the filter. The filter regulatory requirements are driven by tight filtering tolerances of standards such as IEEE P1547.2- 2003 and IEEE 519-1992 [2]. Selecting the current ripple is a trade-off between some factors such as IGBT switching and conduction losses, inductor size, inductor coil, and core losses. Selection of Smaller current ripple resulting in lower IGBT switching and conduction losses, but selection of larger inductor, resulting in larger coil and core losses. Typically, the current ripple is chosen as 15-20% of the rated current [9, 10].

This paper analyses the relation between the L-filter and the current ripple according to the PWM switching technique for single phase grid connected inverters and SVM switching technique for three phase inverters. Based on precise analysis, this paper proposes formulation to get accurate value for inductance in L-filter configuration that satisfies given standard ripple for the injection of current to the grid.

2. ANALYSIS OF CURRENT RIPPLE FOR FULL-BRIDGE SINGLE PHASE INVERTER

In this section the current ripple for full-bridge single phase (FBSP) inverter with PWM switching technique is analysed. Figure 1 shows a FBSP voltage source inverter (VSI) connected to the grid, and its equivalent circuits. Grid voltage v_s is assumed as an ideal sinusoid. As shown in figure 1b the fundamental components of the grid and inverter voltages are assumed to be zero (by using superposition principle). Based on the superposition theory, the response of the L-filter to the composite input can be regarded as the summation of its responses to individual input components. In other words the fundamental component of the inverter (v_{i1}) and grid voltages are considered as a source of fundamental current, while voltage harmonics (v_{iH}) are considered as a source of current ripple. Hence, the fundamental component of the L-filter voltage is also equal to zero.

$$v_{L1} = \sum v_k = v_{i1} - v_s = 0 \quad (1)$$

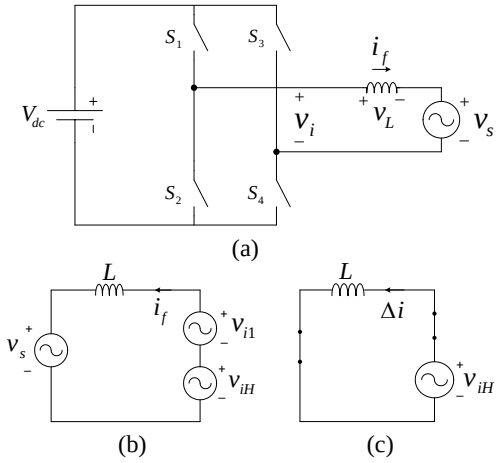


Figure 1: Topology of a FBSP inverter (a), its equivalent circuit (b), and after imposing superposition principle (c).

where v_{i1}, v_{L1} are the fundamental components of inverter and inductor voltage respectively.

Figure 2 shows the unipolar PWM applied to the FBSP inverter. There are three level (values) for the inverter output voltage v_i; (V_{dc}, 0) in first half cycle, and (0, $-V_{dc}$) in second cycle. If the frequency of switching f_s be much higher comparing to the grid frequency f, then the average value of the inverter output voltage $v_{i,av}$, during the switching period T_s can be considered to be constant, and is equal to the fundamental component of inverter output voltage v_{i1}. Note that in the interval ($0 < t < \frac{d_1}{2}T_s$) output voltage of inverter is equal to V_{dc} and so the voltage of inductor as shown in figure 1c is:

$$v_L = (v_f - v_{i1}) = (V_{dc} - v_{i,av}) \qquad (2)$$
$$v_{i,av} = d_1 V_{dc} \ , \qquad 0 < t < \frac{d_1}{2}T_s$$

Thus, the L-filter current by neglecting the fundamental current, has typical waveform as the upper axis in figure 2 in any period of switching. The peak-to-peak value of the L-filter current Δi_{pp} due to the unipolar PWM switching in a period of $\frac{d_1}{2}T_s$ is:

$$\Delta i_{pp} = 2\Delta I_{max} = \frac{(V_{dc} - v_{i,av})}{L}\frac{d_1}{2}T_s \qquad (3)$$

In the case of unipolar PWM the relationship between the modulation index and duty ratio is $d_1 = m$, while for bipolar PWM is $d_1 = \frac{1}{2} + \frac{m}{2}$ (where $m = M_a \sin(\omega t)$). Moreover, when the conditions described above are applied to FBSP inverter, during the interval of ($0 < \omega t < \pi$) equations (4) to (6) can be deduced.

$$v_{i,av}(\omega t) = d_1(\omega t)V_{dc} \qquad (4)$$
$$v_{i,av}(\omega t) = M_a V_{dc}\sin(\omega t) \qquad (5)$$
$$d_1(\omega t) = M_a \sin(\omega t) \qquad (6)$$

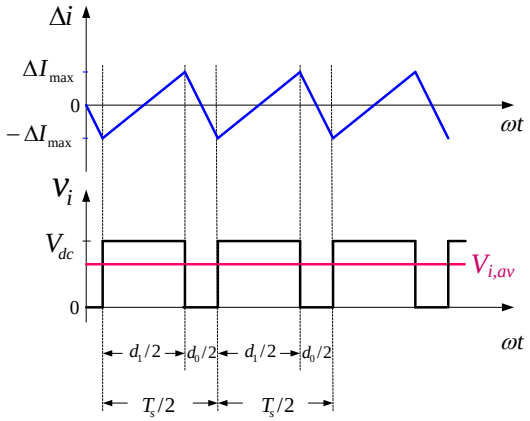


Figure 2: Current and voltage waveforms of a FBSP inverter.

From equations (4) to (6), Δi_{pp} during the interval ($0 < \omega t < \pi$) can be computed by equation (7).

$$\Delta i_{pp}(\omega t) = \frac{V_{dc}T_s}{2L}(1 - M_a \sin(\omega t))M_a \sin(\omega t) \qquad (7)$$

Figure 3 shows the value distribution of Δi_{pp} of grid connected FBSP inverter during the interval ($0 < \omega t < \pi$) for different values of modulation index M_a. Using equation (7), $\Delta i_{pp}(\theta)$ has maximum or minimum magnitude when its angle θ is; $sin^{-1}(1/2M_a)$, $\pi/2$, and $\pi - sin^{-1}(1/2M_a)$. These maximum or minimum values are obtained by $d(\Delta i_{pp})/d\theta = 0$ (where $\theta = \omega t$). In fact value of Δi_{pp} is calculated for each switching period, and in figure 3 it can be assumed that the solid curves are obtained by interpolating and calculating all these calculated points. Since in this case the current and voltage waveforms are symmetrical in each half-cycle, therefore the situation during the interval ($\pi < \omega t < 2\pi$) repeats the same as during the interval ($0 < \omega t < \pi$). As a consequence the maximum value of Δi_{pp} is:

$$\Delta i_{pp,max} = \frac{V_{dc}T_s}{8L} \qquad (8)$$

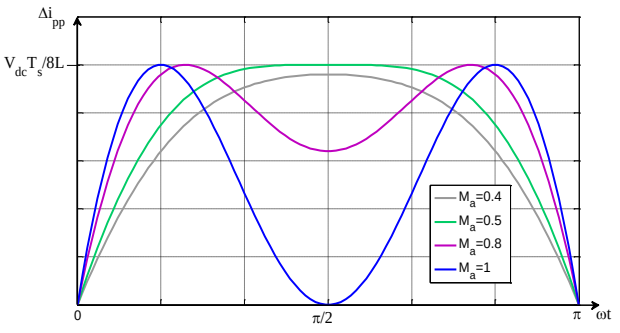


Figure 3: Value of Δi_{pp} during the interval ($0 < \omega t < \pi$) with different values of modulation index M_a for FBSP inverters.

However the position of maximum point changes with respect to the different modulation index.

According to the harmonic standard [2], 15-20% of the rated current is allowable. From equation (8) the maximum current ripple can be computed. As can be seen in this equation, the current ripple depends on the switching frequency, inductance, and the DC link voltage [1]. The switching frequency and DC link voltage are constant, thus the minimum constraint of inductance can be calculated by equation (9).

$$L_{min} = \frac{1}{8} \cdot \frac{V_{dc}}{\Delta i_{pp,max} \cdot f_s} \quad (9)$$

3. ANALYSIS OF CURRENT RIPPLE FOR THREE PHASE INVERTER

In this section the calculation of the current ripple for three phase inverter with SVM switching technique is carried out. Figure 4 shows a three phase grid connected inverter using SVM switching technique during sector (I), while producing the inverter output by combination of two vectors $V_1(100)$ and $V_2(110)$ [11-13]. The peak-to-peak value of the L-filter current Δi_{pp} which results from the SVM can be computed with the same approach but the duty cycle functions are different, as are explained in the next paragraphs.

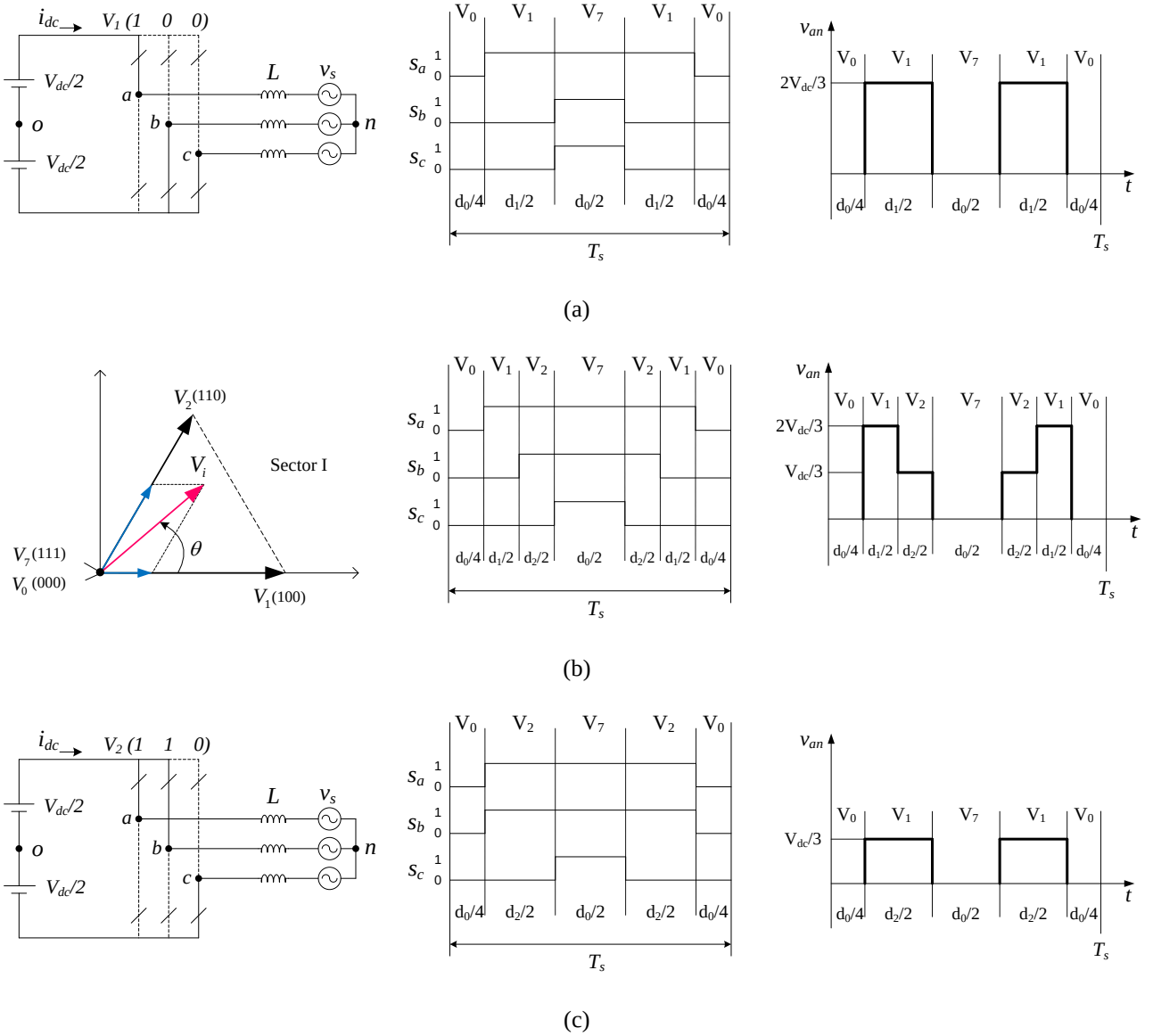
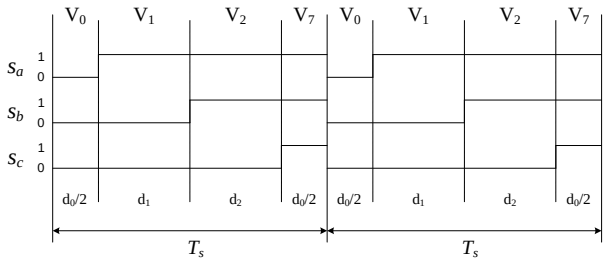
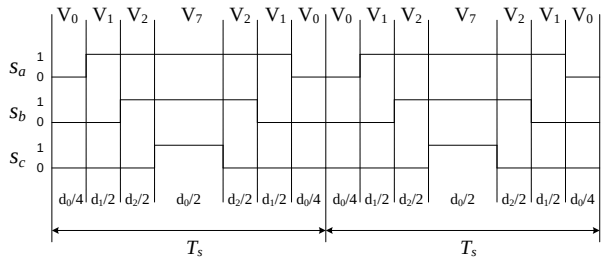


Figure 4: Three phase grid-connected inverter using SVM switching technique in sector I ($0 < \omega t < \frac{\pi}{3}$); (a) circuit, pulses and phase 'a' output voltage (v_{an}) at first switching period of sector (I) when $d_2 = 0$ then only V_1 is applied, (b) vector diagram, pulses and phase 'a' output voltage of the inverter during the sector (I) when d_2 & $d_1 \neq 0$ and the output is obtained by combination of V_1 and V_2, and (c) circuit, pulses and phase 'a' output voltage at the last switching period of sector (I) when $d_1 = 0$ then only V_2 is applied.



(a)



(b)

Figure 5: Typical phase gating signals of; (a) typical asymmetrical switching and (b) symmetrical switching

By considering a balanced load, then the voltages of phases v_a, v_b, v_c with respect to the neutral point (n) chosen such that $v_{an} + v_{bn} + v_{cn} = 0$. The phase voltage v_{an}, as shown in figure 4, has three step values in sector (I); $\frac{2V_{dc}}{3}$, $\frac{V_{dc}}{3}$, and 0 [13].

There are different types of SVM switching that one of them is symmetrical, as an example two techniques are shown in figure 5. For the symmetrical case in each switching period, duty cycles d_1 and d_2 are divided into two equal halves $(d_1/2, d_2/2)$ as shown in figure 5b. In the case of asymmetrical SVM switching, decomposition of the phase voltage switching waveform for SVM to obtain a series of pulses, as shown in figure 6, is a two-step process. As a first step the waveform should be decomposed to obtain stepped pulses in one switching period as shown in figure 7a. Then as a second step this stepped pulse should be further decomposed to obtain pulses, similar to figure 2, as shown in figures 7b and 7c. In the case of symmetrical SVM switching, first half cycle of a switching period should be considered, then the stepped pulse waveform is decomposed to obtain pulses, as shown in figure 7d.

As already mentioned, the inverter average output voltage $v_{an_{av}}$ (for phase 'a') during one switching period T_s can be considered to be constant if the frequency of switching f_s be much higher comparing to the grid frequency f, as shown in figure 7. The average value of voltage in each switching period of sector (I) is:

$$v_{an_{av}} = d_1 \frac{2V_d}{3} + d_2 \frac{V_d}{3} = \frac{V_d}{3}(2d_1 + d_2) \qquad (10)$$

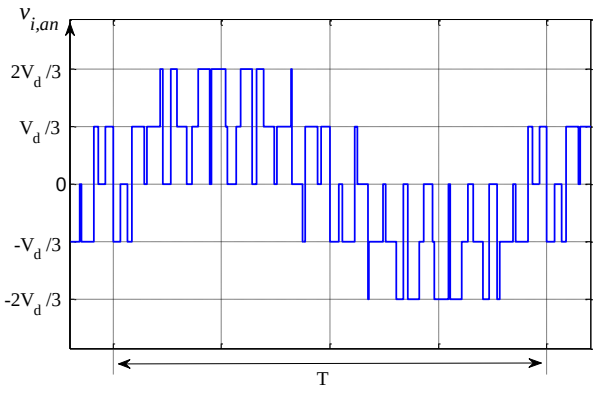


Figure 6: Typical Phase voltage in one phase by SVM switching (v_{ian})

where d_1 and d_2 are the duty cycle of vector V_1 and V_2 in sector (I), respectively. Furthermore d_1 and d_2 in sector (I) can be expressed as:

$$d_1(\omega t) = M_a \sin(\pi/3 - \omega t) \qquad (11)$$
$$d_2(\omega t) = M_a \sin(\omega t) \qquad (12)$$

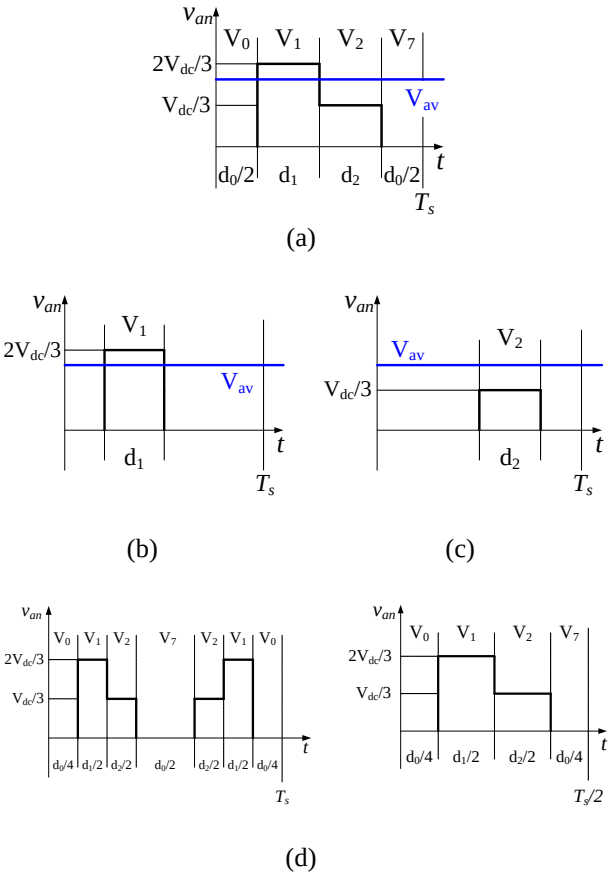


Figure 7: Phase voltage decomposition in one switching period; (a), (b), (c) asymmetrical SVM switching, (d) symmetrical SVM switching

3.1 Current ripple due to vector V_1 in each switching period

The peak-to-peak value of the L-filter current (Δi_{pp1}) due to the vector V_1, as shown in figure 7b, can be calculated in a period of $d_1 T_s$ as:

$$\Delta i_{pp1} = \frac{d_1 T_s}{L}\left(v_{an} - v_{an_{av}}\right) = \frac{d_1 T_s}{L}\left(\frac{2}{3}V_d - v_{an_{av}}\right) = \frac{T_s V_d}{3L} d_1(2 - 2d_1 - d_2) \quad (13)$$

Moreover, by substituting (11) and (12) in above equation during sector (I), Δi_{pp1} can be deduced as:

$$\Delta i_{pp1} = \frac{V_d}{3Lf_s} M_a \sin(\pi/3 - \omega t)\left(2 - 2M_a \sin\left(\frac{\pi}{3} - \omega t\right) - M_a \sin(\omega t)\right), \quad (0 < \omega t < \frac{\pi}{3}) \quad (14)$$

Figure 8 shows the magnitude distribution of Δi_{pp1} of phase 'a' during the interval $(0 < \omega t < \pi/3)$, for different values of modulation index M_a. As one can see in figure 8 the ripple $\Delta i_{pp1}(\omega t)$ has its maximum value when $\omega t = 0$ and the modulation index is $M_{a,r\,max} = 1/\sqrt{3}$. It means, in phase '$a$' the maximum current ripple occurs when the vector V_i is collinear with V_1 in figure 4b. In this moment the duty cycle related to the vector V_2 is zero ($d_2 = 0$), and the resultant phase voltage is in accordance with figure 4a. The $M_{a,r\,max} = 1/\sqrt{3}$ is obtained by $d(\Delta i_{pp1})/dM_a = 0$ and at $\omega t = 0$ as:

$$M_{a,r\,max} = \frac{1}{2\sin\left(\frac{\pi}{3} - \omega t\right) + \sin(\omega t)}\bigg|_{\omega t = 0} = \frac{1}{\sqrt{3}} \quad (15)$$

Therefore the maximum value of Δi_{pp1} is given by:

$$\Delta i_{pp1,max} = \frac{V_{dc}}{6Lf_s} \quad (16)$$

3.2 Current ripple due to vector V_2 in each switching period

The peak-to-peak value of the filter inductor current (Δi_{pp2}) due to the vector V_2, as shown in figure 7c, can be calculated in a period of $d_2 T_s$ just like that for V_1 and is given by equation (17).

$$\Delta i_{pp2} = \frac{d_2 T_s}{L}\left(\frac{V_d}{3} - v_{an_{av}}\right) = \frac{T_s V_d}{3L} d_2(1 - 2d_1 - d_2) \quad (17)$$

By substituting (11) and (12) in (17), Δi_{pp2} during sector (I) can be written as:

$$\Delta i_{pp2} = \frac{V_d}{3Lf_s} M_a \sin(\omega t)\left(1 - 2M_a \sin\left(\frac{\pi}{3} - \omega t\right) - M_a \sin(\omega t)\right), \quad (0 < \omega t < \frac{\pi}{3}) \quad (18)$$

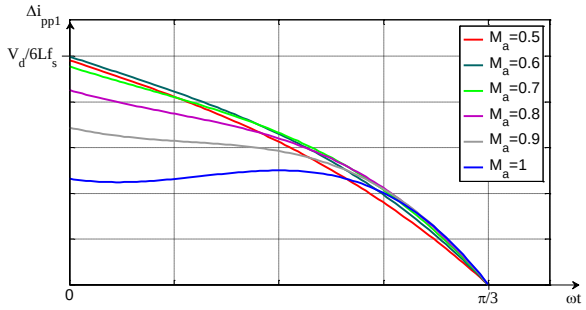


Figure 8: Magnitude distribution of Δi_{pp1} in sector I ($0 < \omega t < \frac{\pi}{3}$).

Figure 9 shows the magnitude distribution of Δi_{pp2} of phase 'a' during the period $(0 < \omega t < \pi/3)$, for different values of modulation index M_a. Finally the peak-to-peak value of Δi_{pp} due to both vectors V_1 and V_2, as shown in figure 10, can be calculated as equation (19).

$$\Delta i_{pp} = \Delta i_{pp1} + \Delta i_{pp2} \quad (19)$$

One can see the result for the maximum value of total ripple $\Delta i_{pp,max}$ is the same as maximum ripple due to V_1 that is:

$$\Delta i_{pp,max} = \Delta i_{pp1,max} = \frac{V_{dc}}{6Lf_s} \quad (20)$$

Equation (20) is true for asymmetrical SVM switching. For symmetrical SVM switching the duty cycles d_1 and d_2 are split in half and hence:

$$\Delta i_{pp,max} = \Delta i_{pp1,max} = \frac{V_{dc}}{12\,Lf_s} \quad (21)$$

Basically to design the L-filter the worst case must be considered; it means the maximum ripple should be considered. The elements in this analysis assumed to be ideal. It would be useful to perform a similar analysis by considering real elements. In addition the analysis of unbalancing based on symmetrical components (positive-, negative-, and zero-sequence components) would be very interesting.

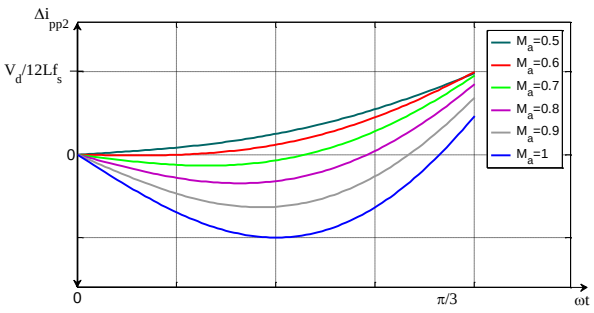


Figure 9: Magnitude distribution of Δi_{pp2} in sector I ($0 < \omega t < \frac{\pi}{3}$).

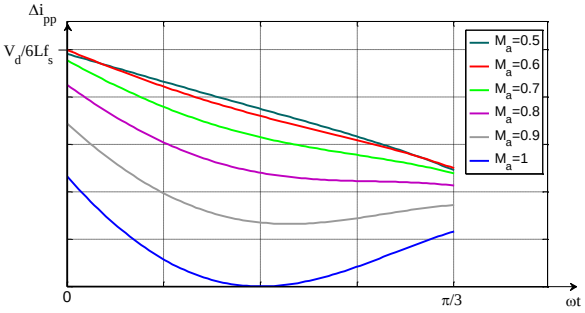


Figure 10: Magnitude distribution of Δi_{pp} in sector I $(0 < \omega t < \frac{\pi}{3})$.

4. CONCLUSION

Switching current ripple for single phase and three phase inverter with PWM and SVM switching techniques respectively have been analysed. Variation of the maximum switching current ripples during different switching periods over the fundamental period of the grid voltage is considered. Peak of these variations give overall maximum switching current ripple which is very important and essential to be used for the accurate estimation of the ripple and hence to calculate the value of L-filter required meeting the current ripple specification. For many years the best way to find an optimum value for filter inductance in order to have the best result was the trial and error method. The calculation in this paper is very useful to get accurate value for inductance to design L-filter configuration, and also to get necessary intermediate value for inductance to design LCL-filter configuration.

5. REFERENCES

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